FIG_1 (prior art)

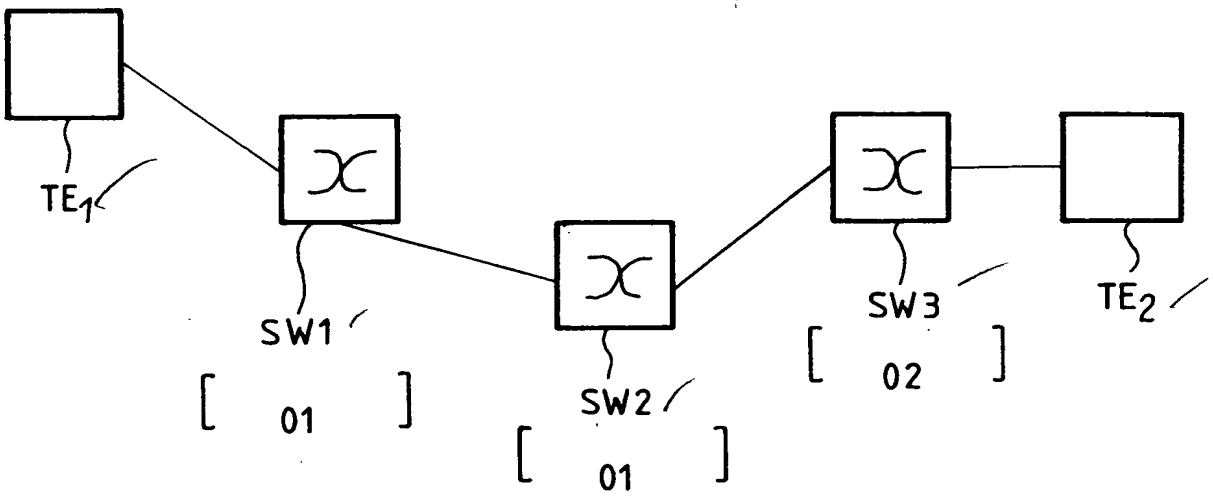
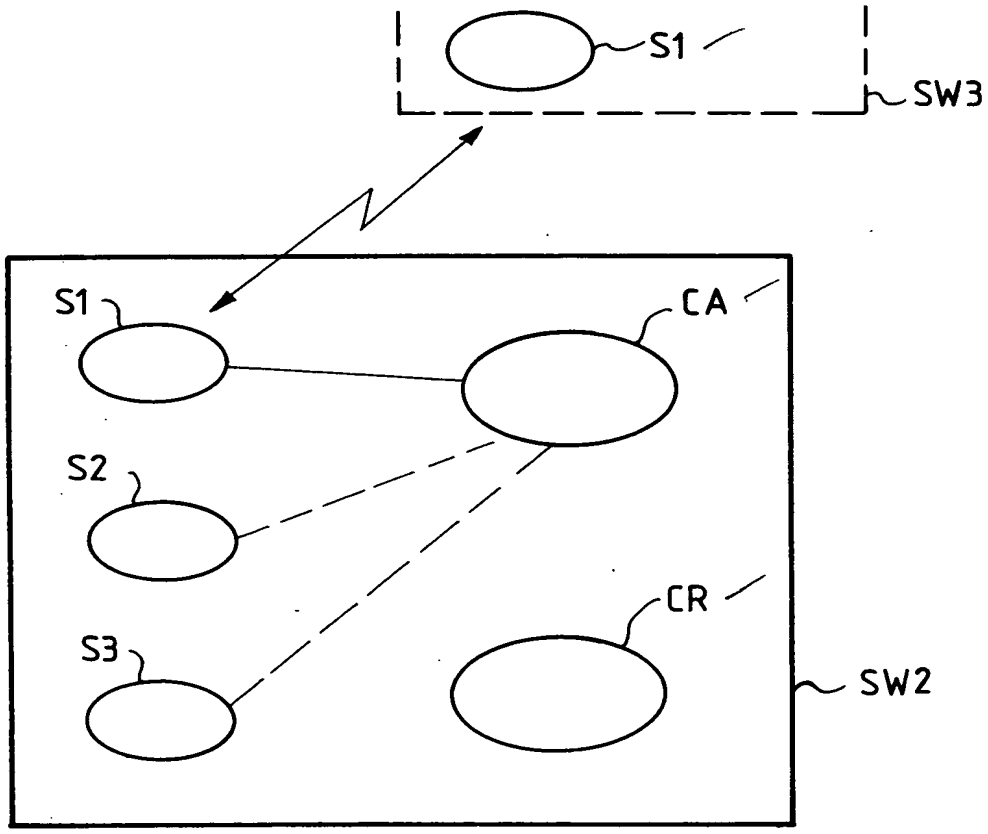


FIG_2 (prior art)



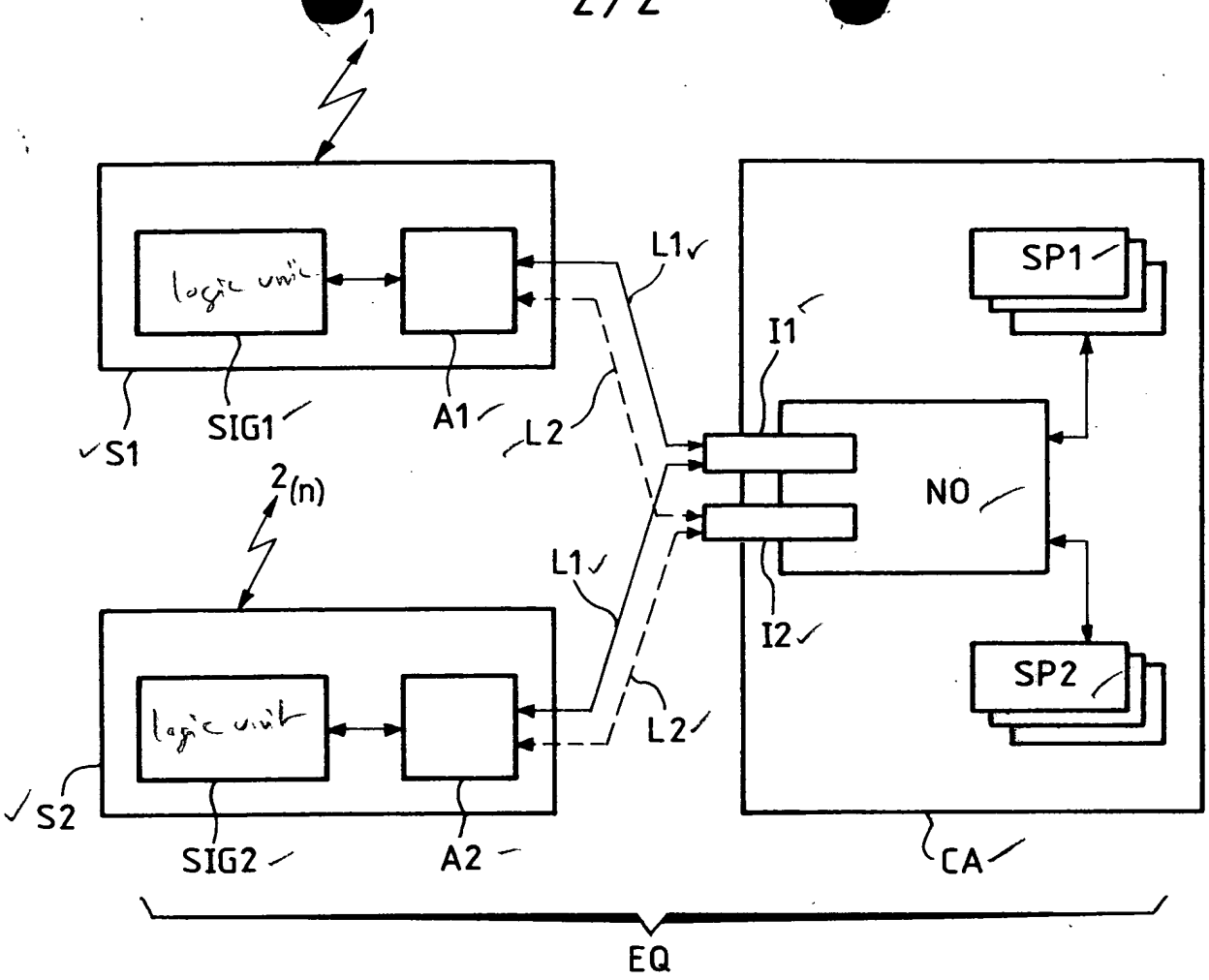

1
logic unit
L1
SP1
I1
S1
SIG1
A1
L2
2(n)
NO
L1
I2
SP2
logic unit
L2
S2
SIG2
A2
CA
EQ

FIG_3